REMARKS/ARGUMENTS

Reconsideration of the application, in view of the above amendments and the following remarks is respectfully requested.

The Examiner rejects Claim 4 under 35 U.S.C § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that the claim is indefinite because it is unclear why the impedance of the first node is higher than it self's impedance.

Claim 4 has been amended in order to correct the error and now recites that the error amplifier has a higher impedance of the first node and that the compensating compacitor is coupled to this first node. Thus, it covers the alternative to Claim 3.

The Examiner rejects claims 1, 3, 4, 6-8, 10, 11, 19 and 20 under 35 U.S.C. § 102(e) as being anticipated by Noda et al. The Examiner states that Noda's FIGURE 1 shows a method of stabilizing two current loops within a circuit comprising providing a main current loop, supplying current to a load, controlling current to the load, an error amplifier for the main current loop coupled to an error amplifier for the sensing loop such that the capacitance of each loop is isolated from that of the other loop.

We can not agree. The circuit presented in Noda is a circuit that has a positive feedback loop from the output V_{IN} into the Va1 input. Taking, for example, the loop 18, starting at Va1, we can see that the signal would go from Q16 to Q19 to Q20 to Q22 to Q11 to Q13 and that this path would provide for four (4) inversions. That is, a -1 from Q16, a +1 from Q19, a -1 from Q20, a -1 from Q22, a -1 from Q11, a +1 from Q19. Therefore, Noda provides a positive feedback loop. The present invention is directed to negative feedback loops. Accordingly, Claims 1, 6 and 14 have been amended in this respect.

The Examiner rejects claims 1-5 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Larson et al. The Examiner states that Lee's FIGURE 2 shows a method comprising providing a main current loop, a sensing loop such that the capacitance of each loop is isolated from the other loop. The Examiner states that FIGURE 2 shows all limitations to the claim except for the step of providing a compensating capacitor for the main loop. The Examiner states that Larson's FIGURE 2 shows a circuit having a compensating compacitor C_{out} coupled to the output of the main loop in order to stabilize the output voltage and concludes that it would have been obvious to one who having ordinary skill in the art to add a compensating capacitor to the output of Lee's main loop for the purpose of stabilizing the output voltage.

It is inappropriate to combine Lee's circuit and Larson's circuit because Lee's uses a PMOS device P1 to provide current to the load and Larson's uses a NMOS for to provide load current. Depending whether one uses and NMOS or PMOS transistor to provide load current, the compensation required changes and therefore it is not obvious to just combine both compensation schemes. A PMOS LDO requires Miller compensation given that the PMOS requires an additional gain stage in the loop and requires one to achieve pole splitting and an NMOS LDO requires a different type of compensation since the NMOS does not add any significant amount of gain to the loop. The circuit shown in Larson is missing the compensation capacitor for the sensing loop composed of comparator 9 and NMOS device 10 so it is not possible to determine how this loop has been stabilized. Lee utilizes two different feedback loops, one through P3 and the other one through P2, which inevitably creates two paths in which one will have positive feedback and the other will have negative feedback. However, Lee only shows a single capacitor P_{cc} that is implementing Miller compensation through the loop that comprises the comparator 1 (18) and device P1. No capacitor is shown to stabilize the loop that comprises comparator 2. Therefore, it is not known how they stabilize both loops.

The Examiner rejects claims 5, 12, 13, 14 and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Noda et al. The Examiner states that Noda failed to teach the main loop comprises a LDO voltage regulator but that this is notoriously well known in the art.

As stated above, the present invention applies to negative feedback loops and the main claims have been amended in this respect.

The Examiner states that claims 9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, these claims have been converted into independent claims.

Accordingly, Applicant's believe that the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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